REMARKS

The Applicant wishes to thank the Examiner for his examination of the present application. Please note that the applicant has made minor corrections to the specification. No new matter has been added with these corrections. Applicant has also added additional dependent claims 20-24. Again, no new matter has been added. Claim 19 has been cancelled. Claims 1-18 and 20-24 are currently pending in this application. The claims have been amended to more clearly describe the novelty of the invention.

SPECIFICATION

The Applicant notes that the paragraph beginning at page 15 line 14 of the specification has been amended to correct some typographical errors. For example, the DMR element was incorrectly labeled with number 1110, whereas the DMR is properly referenced by number 1010. Additionally, the terminology used to describe the demultiplexing process was incorrectly referenced as a multiplexing process. The device marked 1040 in Fig. 10 performs both demultiplexing and multiplexing depending on whether the data is being compressed or decompressed respectively. However, the text of the paragraph beginning at page 15 line 14 references demultiplexing and therefore element 1040 is referred to as a demultiplexor during the process of compression.

DRAWINGS

Applicant has updated the drawings in accordance with the Examiner's suggestion. A clean copy of the amended figures along with a copy of the figures marked in red accompanies this response. Fig. 2 now includes the words "Digital Video System Chip" inside of each box labeled 15. Fig. 7A now includes the word "Bus" for element 810. Fig. 8 has been amended such that the blocks 650A-650C each include the word "CODEC." Fig. 10 now includes the label "De-Mux" in each box labeled 1040 It is believed that the drawings are now in the proper form and the objection is overcome.

35 U.S.C. 112

Claim 19 was rejected based upon 35 U.S.C. 112, second paragraph for indefiniteness. Claim 19 has been cancelled.

35 U.S.C. 102(e)

The office action rejects claim 1-4 and 7-19 as being anticipated by published patent application (US 2002/0057844) to Sirohey et al.

The present invention as claimed in independent claim 1 is directed to a scalable motion image compression system. The system allows for decomposing a digital video stream through a decomposition module where the digital video stream is transmitted in real-time at a transmission rate. The decomposition module decomposes the digital video stream into a number of component parts and forwards the decomposed video stream to a compression module. The compression module contains a plurality of compression blocks that each process in parallel separate component parts of the digital video stream.

The Sirohey reference is directed an image data management system that decomposes and tessellates sub-band blocks of an image for easy transmission and distribution as defined in the Abstact. The system is preferably used for the storage and transmission of medical image, such as a portion of an MRI image See page 2 paragraph 36. It should be noted that the Sirohey reference is applicable to a compression of individual images (for example, see paragraph 45), whereas the present invention is directed to a scalable system for compression of a motion image video stream. As a result, independent claim 1 clearly distinguishes the Sirohey reference and is therefore allowable.

Additionally, as shown in Fig. 1 of the Sirohey reference, the image management system includes a single compression/decompression interface 20. The text of the Sirohey reference at paragraph 39 states that a compression/decompression library is coupled to interface 20 and that the library stores the routines and algorithms used by the interface. Thus, the interface 20 accesses the software routines and processes the image according to the algorithm. Nowhere in the reference is the compression/decompression module described as containing a plurality of compression units that operate in parallel to process sections of the decomposed image as required by the claims.

Further still, the Sirohey reference does not teach a system that decomposes the video stream into component parts and passes the component parts to a compression module at the transmission rate of the video stream wherein the component parts are processed in parallel. The office action suggests that this is shown in Fig. 15, however Fig. 15 is directed to the process flow of data for a single image. The Fig. does not show multiple compression units. In fact, the process flow of Fig. 15 cannot process a digital video stream in substantially real-time as required by independent claim 1, since each

subsequent level of the wavelet decomposition must wait until the previous level's decomposition is complete. Thus, the system would fail with a digital video image stream.

Therefore, independent claim 1 is allowable over the art of record. Additionally, dependent claims 2-18 and 20-24 each depend from independent claim 1 and add at least one additional limitation. The dependent claims are allowable for at least the same reasons as independent claim 1.

35 U.S.C. 103

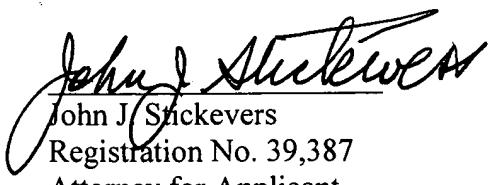
With regard to the 35 U.S.C. 103 rejections of dependent claims 5 and 6, the Sirohey reference does not teach each and every limitation of independent claim on which claims 5 and 6 depend. As a result, claims 5 and 6 can not be obvious in view of the Sirohey reference and are therefore, allowable over the art of record.

It is believed the application is now in condition for allowance. Reconsideration of the claims and issuance of a notice of allowance are respectfully requested.

If any matter arises which may expedite issuance of a notice of allowance, the Examiner is requested to call the undersigned, at the telephone number given below.

It is believed no extension is required for this application, but if an extension is required, the applicant respectfully petitions for such an extension. Please charge deposit account number 19-4972 for the extension fees. If any additional fees are required for the timely consideration of this application, please charge deposit account number 19-4972.

Respectfully submitted,



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02418/00125 495109.1

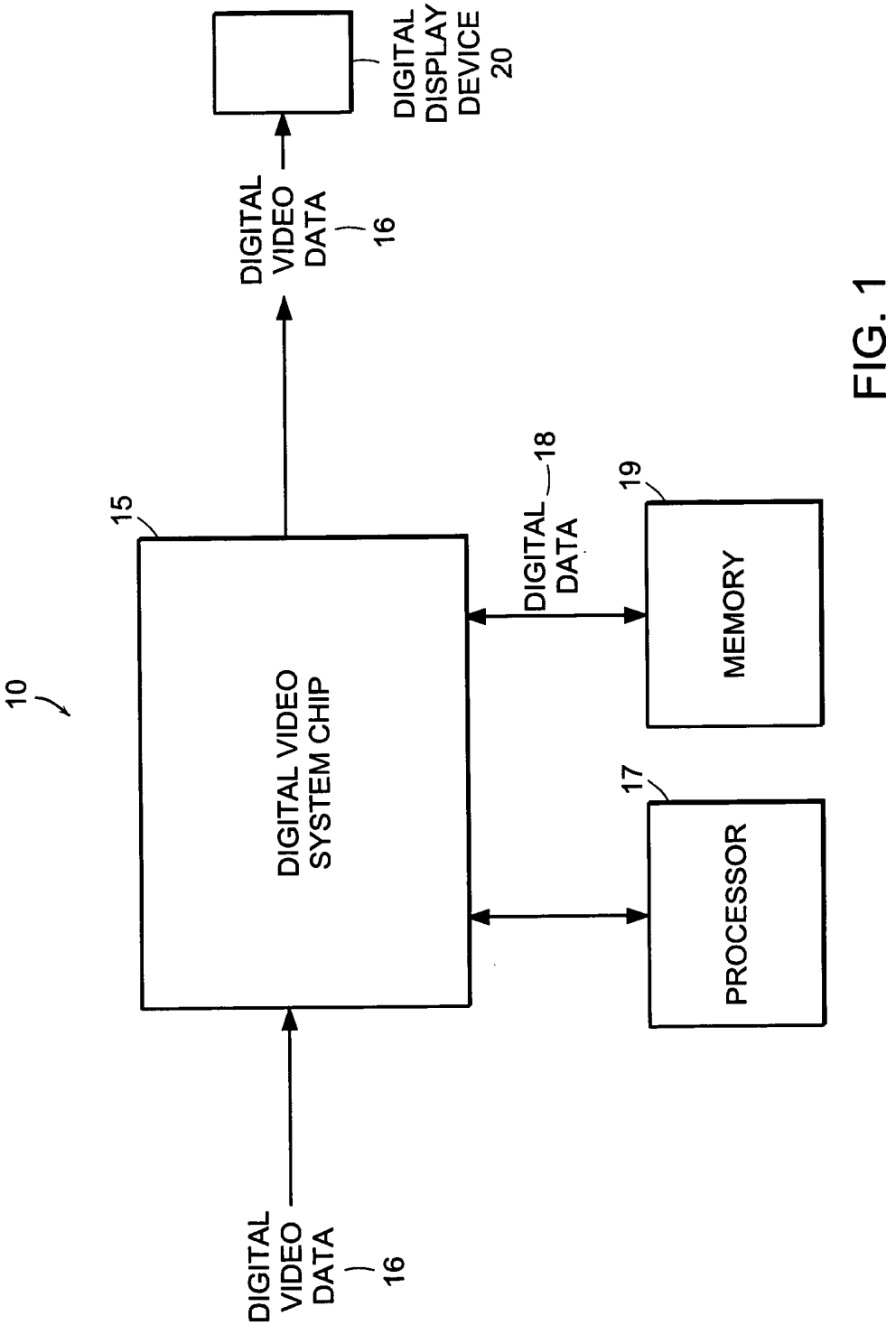

FIG. 1

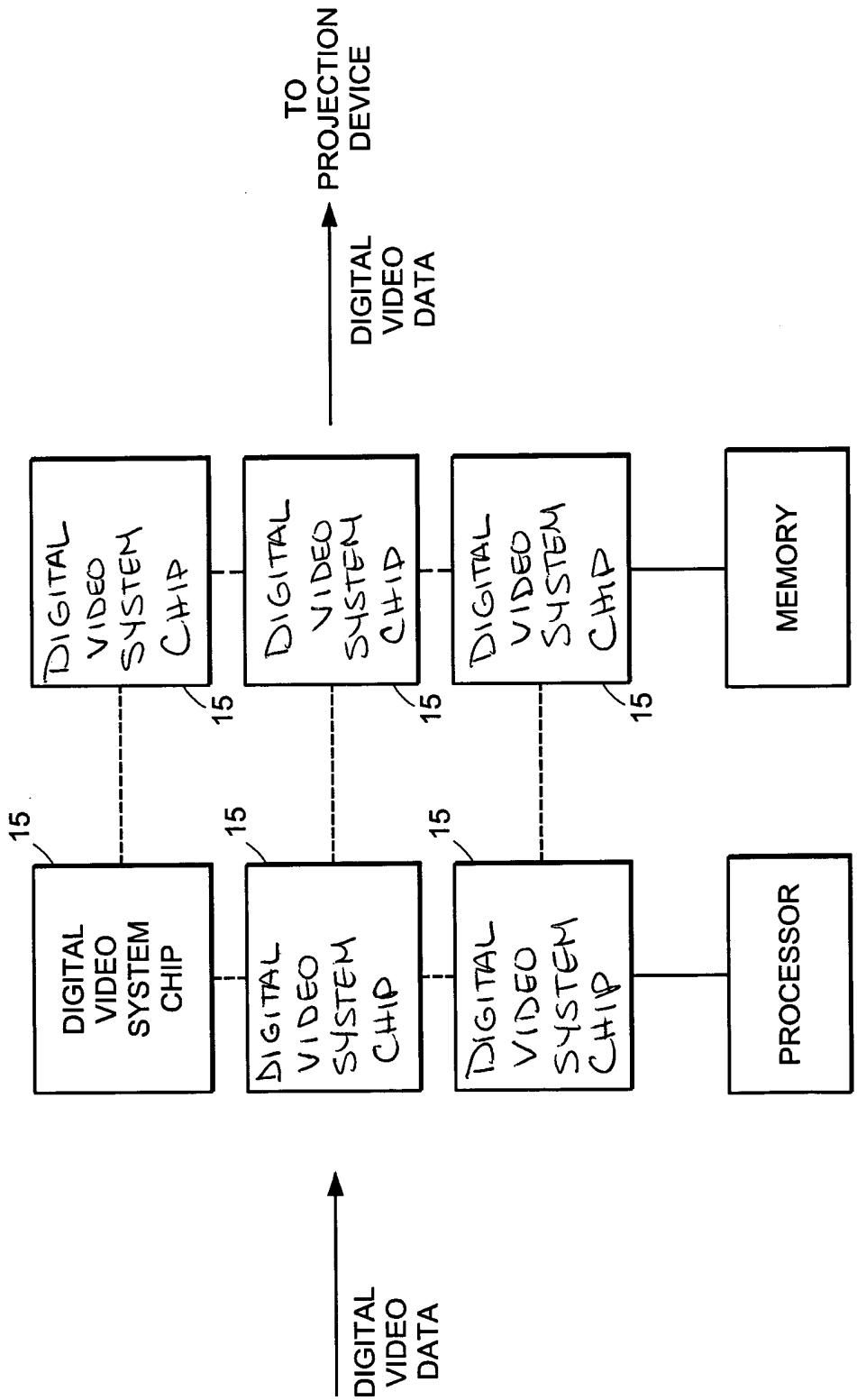
TO PROJECTION DEVICE
DIGITAL VIDEO DATA
DIGITAL VIDEO SYSTEM CHIP
DIGITAL VIDEO SYSTEM CHIP
DIGITAL VIDEO SYSTEM CHIP
MEMORY
15
15
15
15
15
15
DIGITAL VIDEO SYSTEM CHIP
DIGITAL VIDEO SYSTEM CHIP
DIGITAL VIDEO SYSTEM CHIP
PROCESSOR
DIGITAL VIDEO DATA

FIG. 2

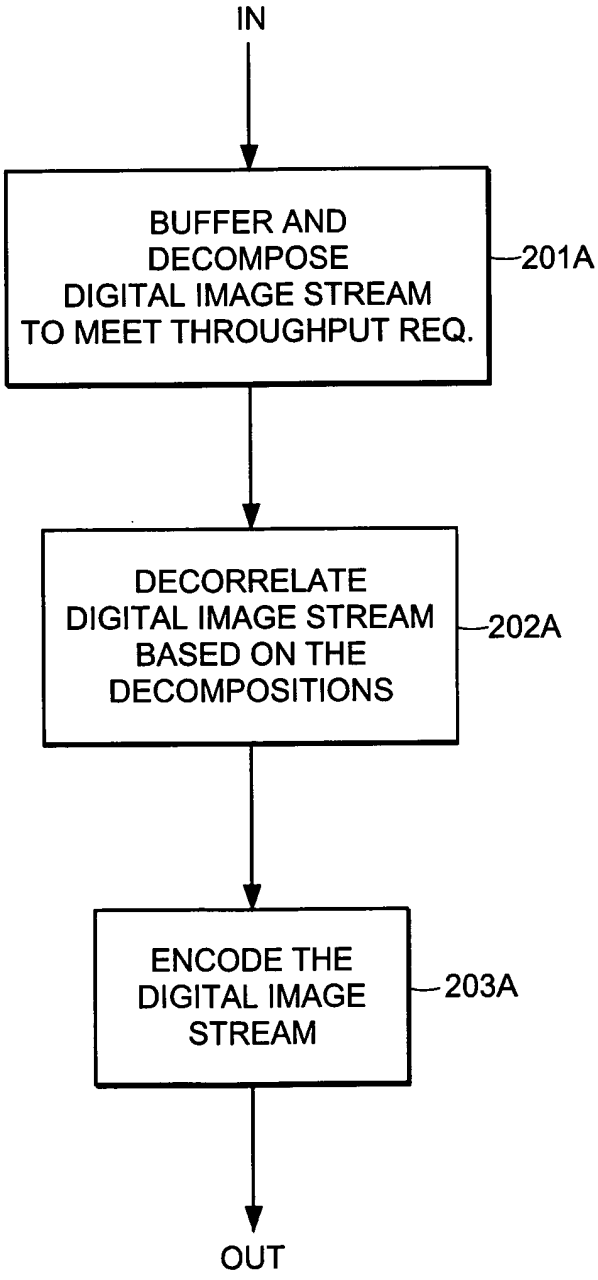
IN
BUFFER AND DECOMPOSE DIGITAL IMAGE STREAM TO MEET THROUGHPUT REQ.
201A
DECORRELATE DIGITAL IMAGE STREAM BASED ON THE DECOMPOSITIONS
202A
ENCODE THE DIGITAL IMAGE STREAM
203A
OUT

FIG. 2A

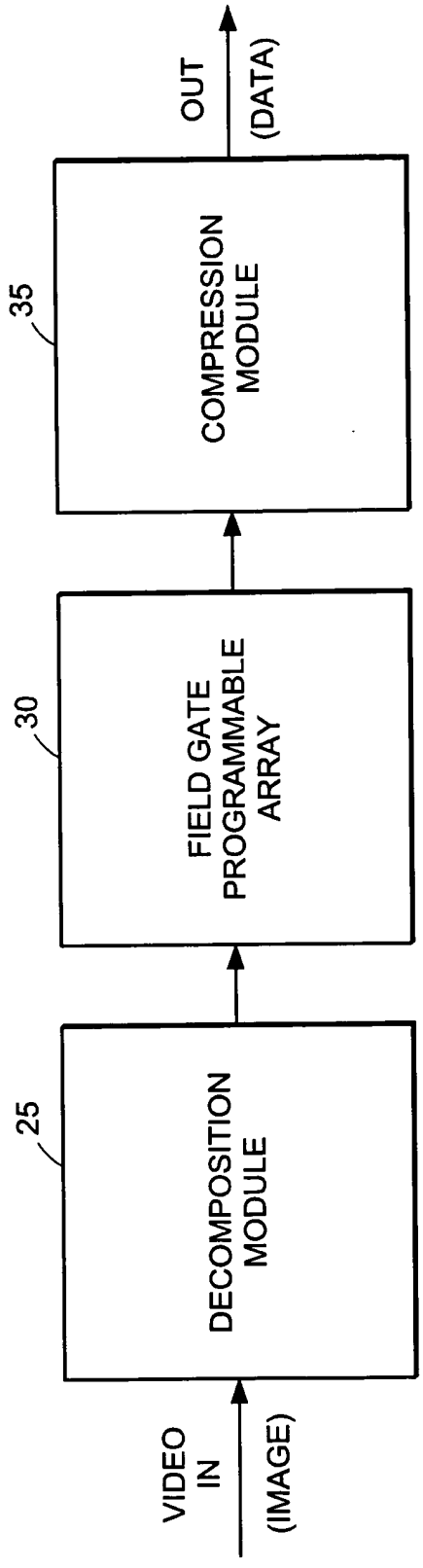
VIDEO IN
(IMAGE)
25
DECOMPOSITION MODULE
30
FIELD GATE PROGRAMMABLE ARRAY
35
COMPRESSION MODULE
OUT
(DATA)

FIG. 2B

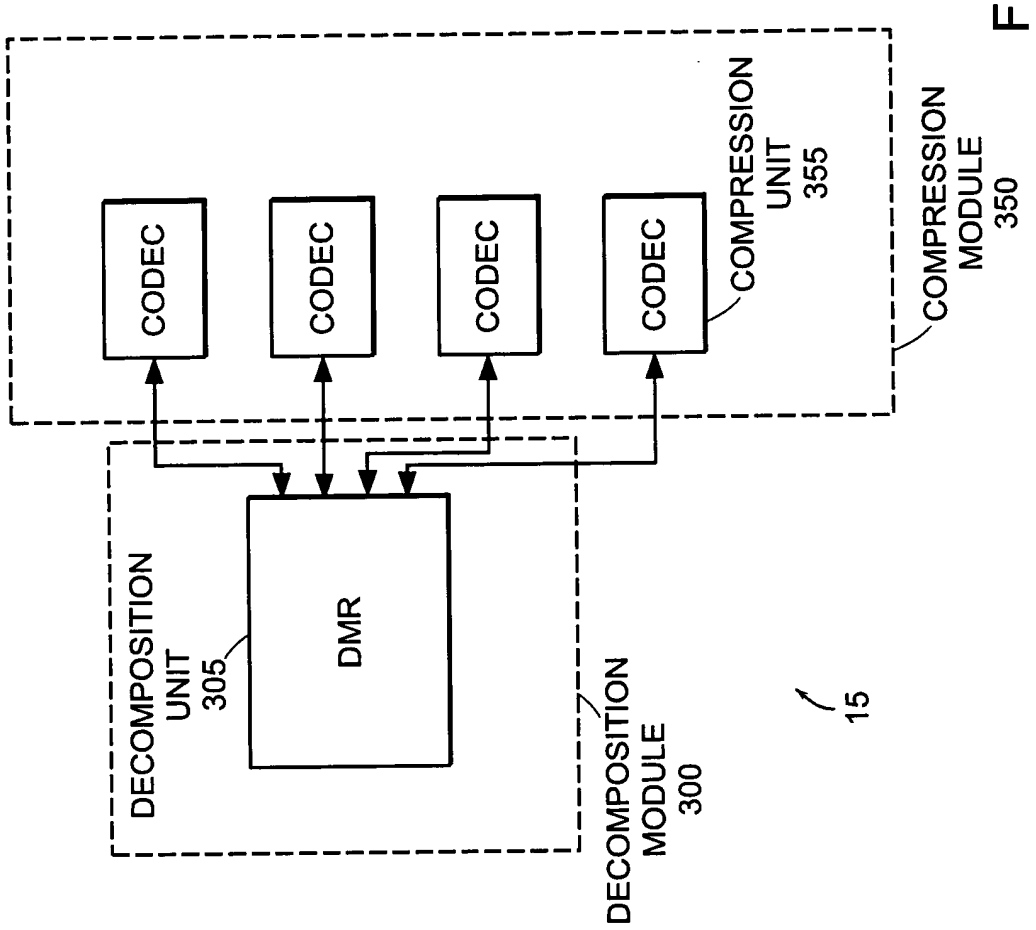
CODEC
CODEC
CODEC
CODEC
COMPRESSION UNIT 355
COMPRESSION MODULE 350
DECOMPOSITION UNIT 305
DMR
DECOMPOSITION MODULE 300
15

FIG. 3

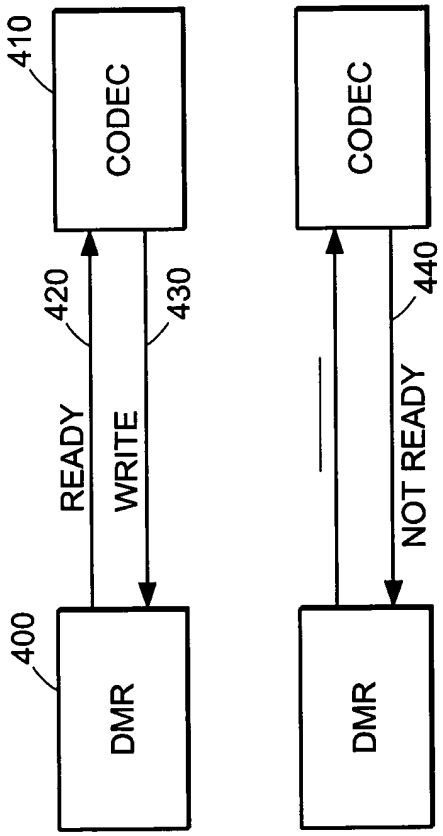

FIG. 4

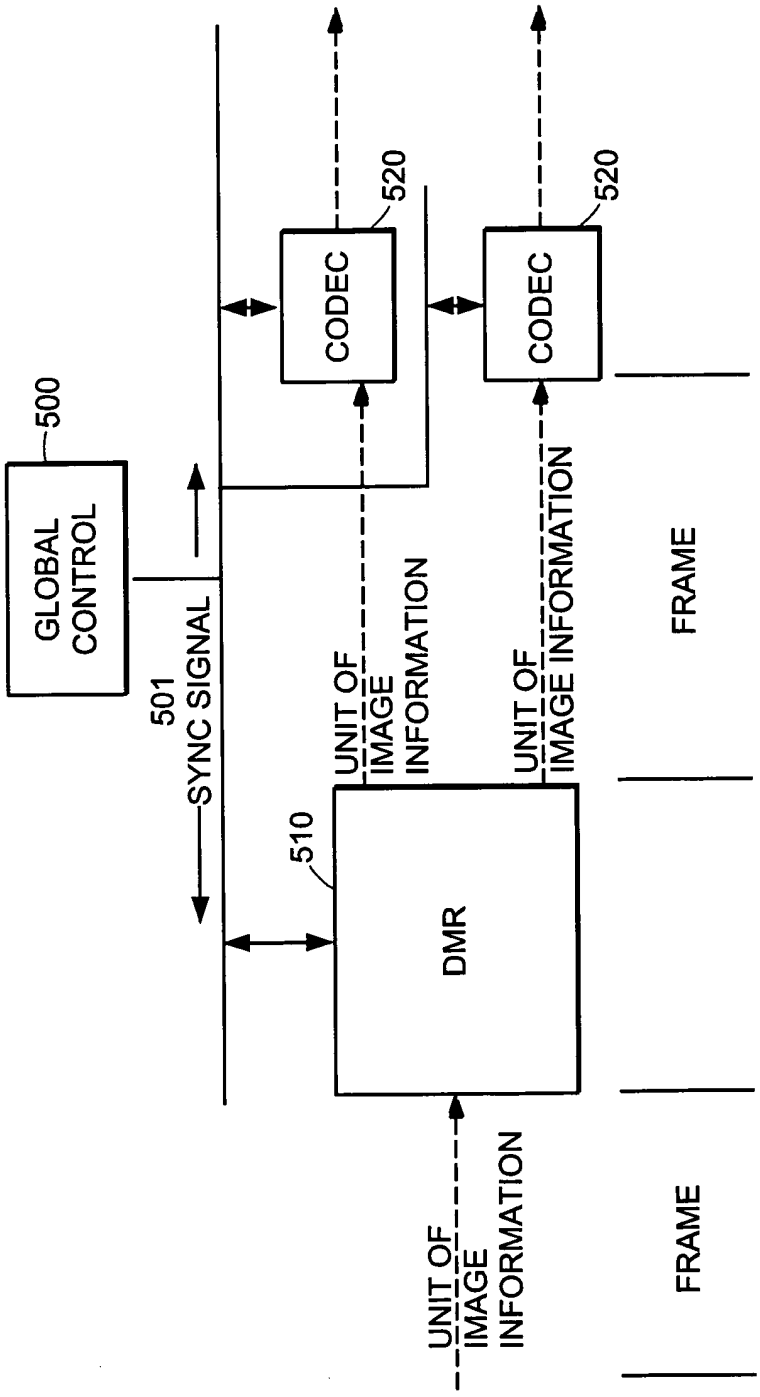
500
GLOBAL CONTROL
501
SYNC SIGNAL
CODEC
520
CODEC
520
UNIT OF IMAGE INFORMATION
UNIT OF IMAGE INFORMATION
510
DMR
UNIT OF IMAGE INFORMATION
FRAME
FRAME

FIG. 5

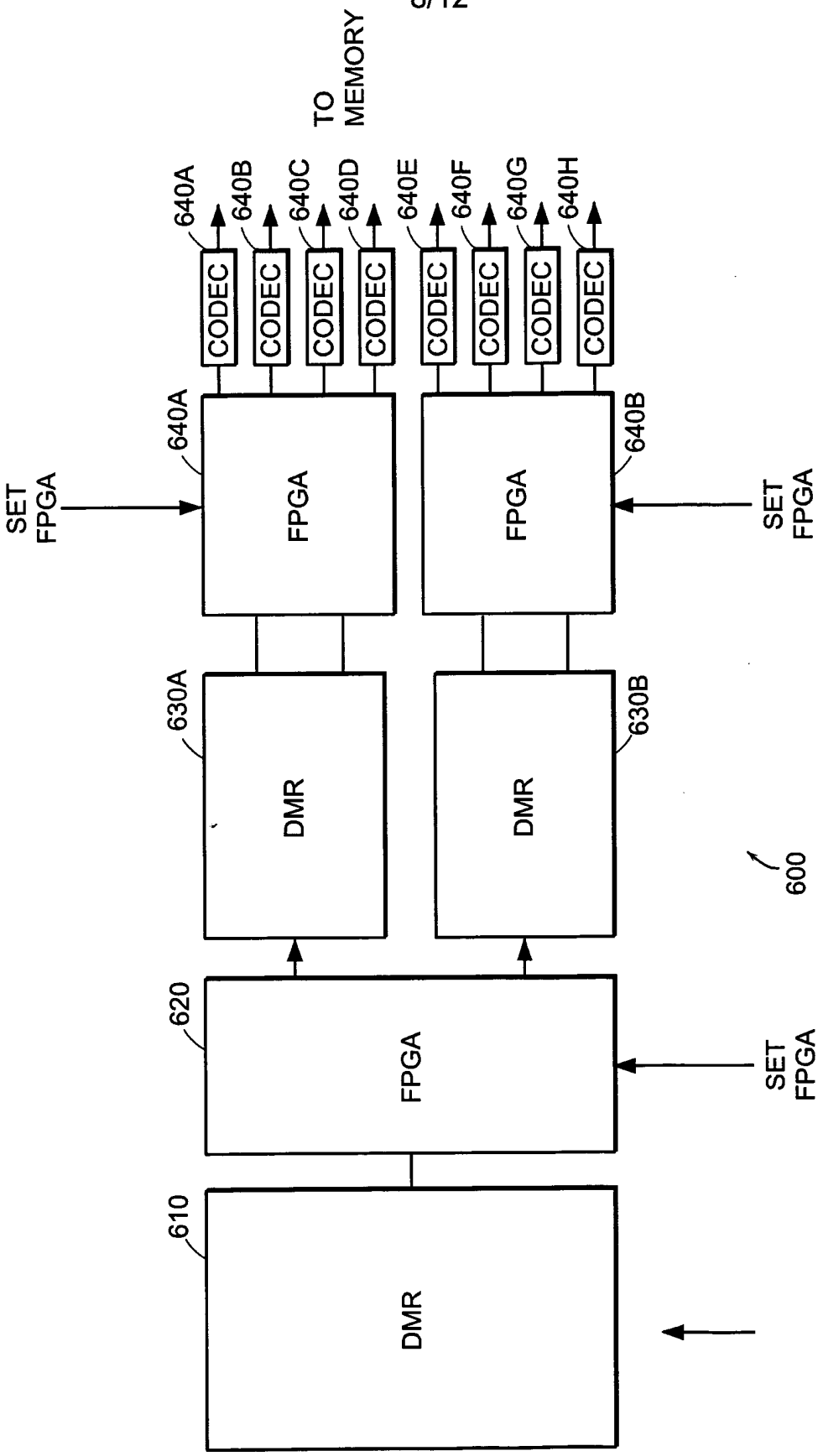
TO MEMORY
640A
640B
640C
640D
640E
640F
640G
640H
CODEC
CODEC
CODEC
CODEC
CODEC
CODEC
CODEC
CODEC
640A
640B
SET FPGA
FPGA
FPGA
SET FPGA
630A
630B
DMR
DMR
620
FPGA
SET FPGA
610
DMR
600

FIG. 6

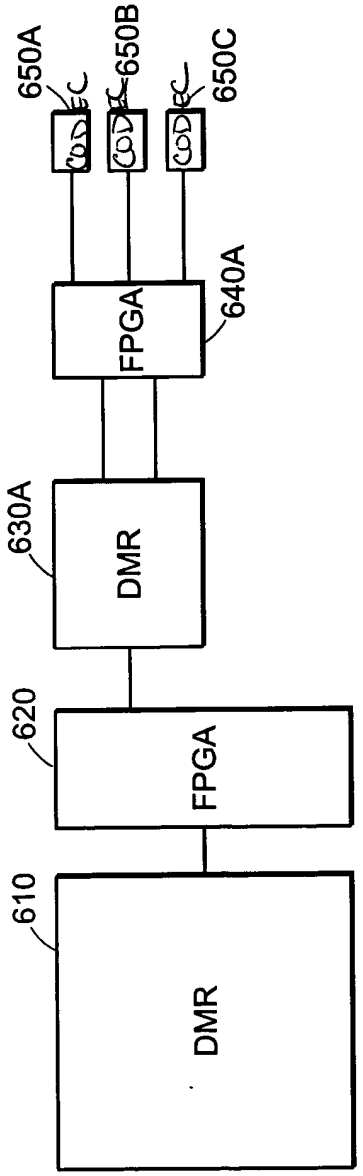
650A
650B
650C
CODEC
CODEC
CODEC
640A
FPGA
630A
DMR
620
FPGA
610
DMR

FIG. 7A

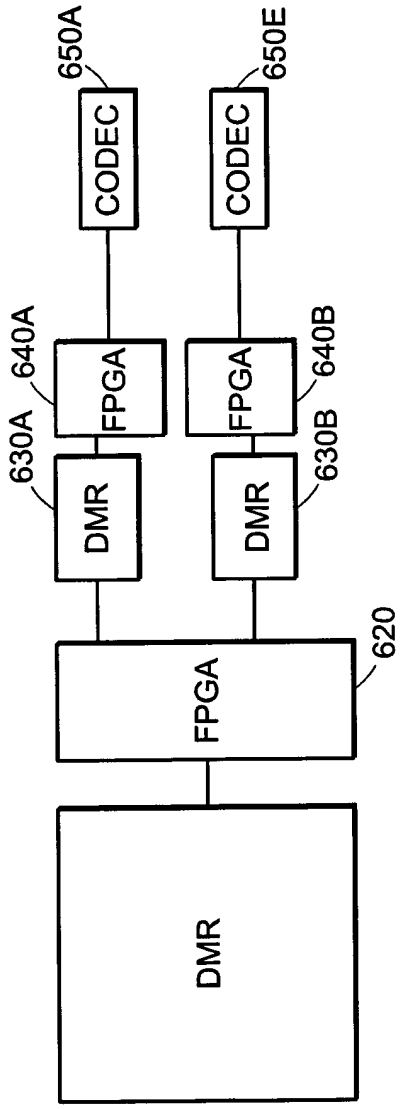
650A
650E
CODEC
CODEC
640A
FPGA
FPGA
640B
630A
DMR
DMR
630B
620
FPGA
DMR

FIG. 7B

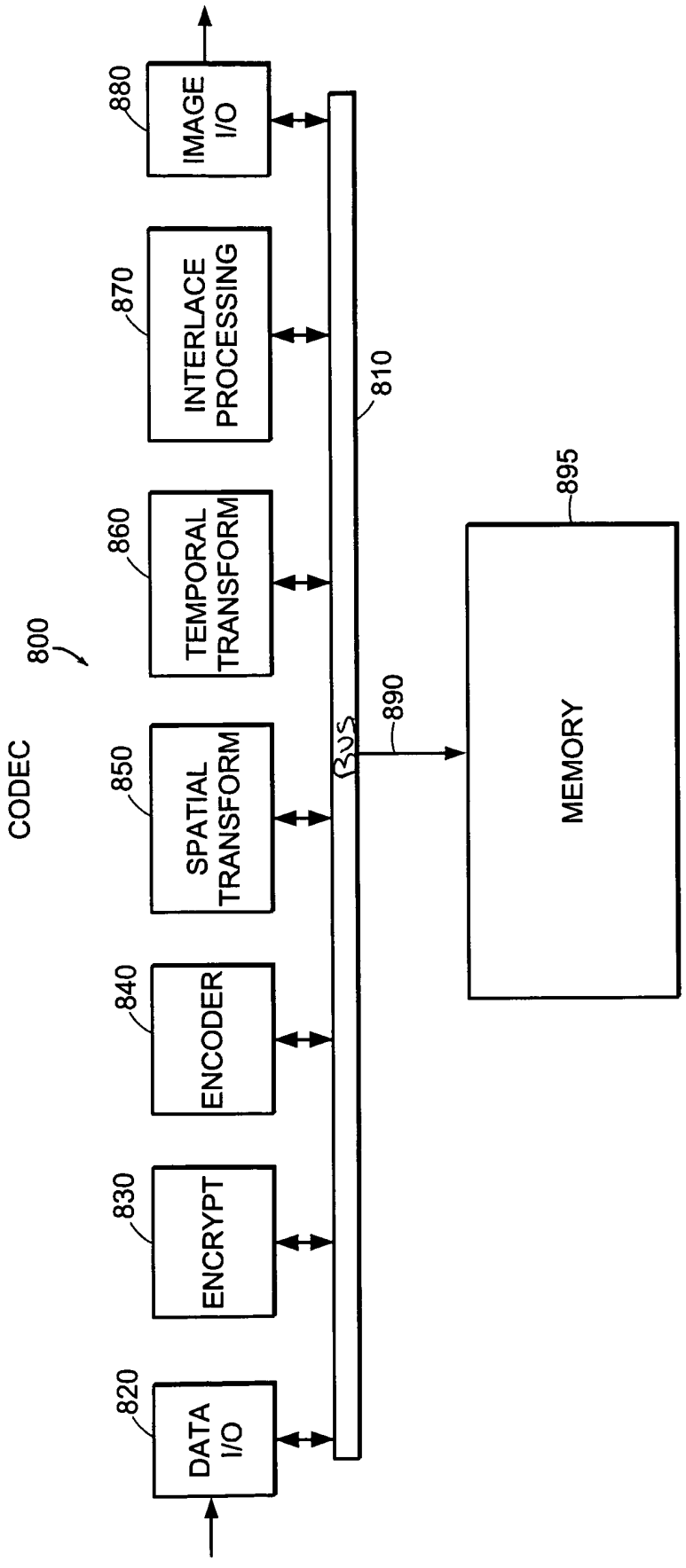
CODEC
800
880
IMAGE I/O
870
INTERLACE PROCESSING
860
TEMPORAL TRANSFORM
850
SPATIAL TRANSFORM
840
ENCODER
830
ENCRYPT
820
DATA I/O
810
Bus
890
895
MEMORY

FIG. 8

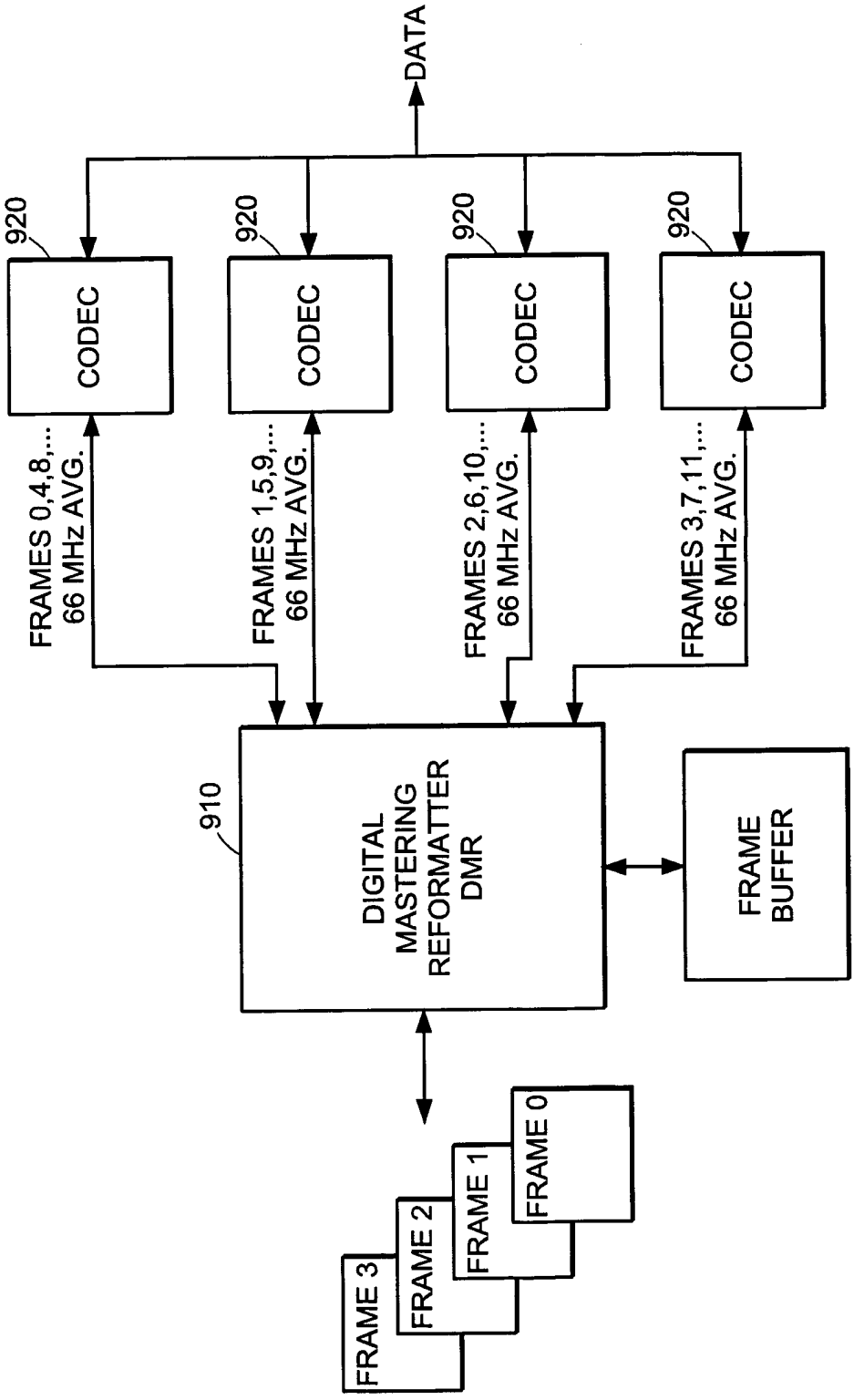
DATA
920
CODEC
920
CODEC
920
CODEC
920
CODEC
FRAMES 0,4,8,... 66 MHz AVG.
FRAMES 1,5,9,... 66 MHz AVG.
FRAMES 2,6,10,... 66 MHz AVG.
FRAMES 3,7,11,... 66 MHz AVG.
910
DIGITAL MASTERING REFORMATTER DMR
FRAME BUFFER
FRAME 0
FRAME 1
FRAME 2
FRAME 3

FIG. 9

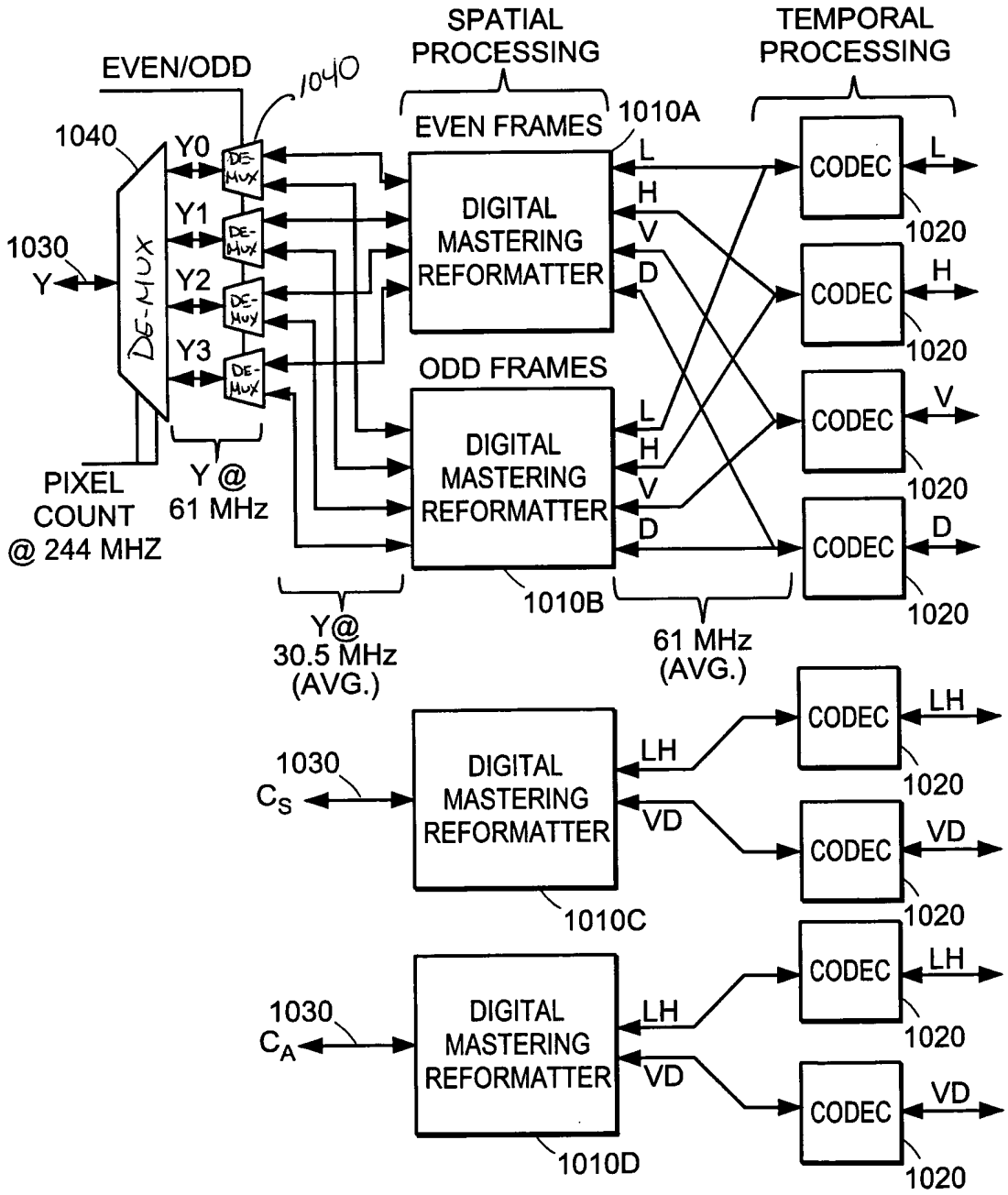
SPATIAL PROCESSING
TEMPORAL PROCESSING
EVEN/ODD
1040
1040
Y0
Y1
Y2
Y3
DE-MUX
DE-MUX
DE-MUX
DE-MUX
DE-MUX
1030
Y
PIXEL COUNT @ 244 MHZ
Y @ 61 MHz
EVEN FRAMES
1010A
DIGITAL MASTERING REFORMATTER
L
H
V
D
ODD FRAMES
DIGITAL MASTERING REFORMATTER
1010B
Y@ 30.5 MHz (AVG.)
61 MHz (AVG.)
CODEC
1020
1030
C_S
DIGITAL MASTERING REFORMATTER
LH
VD
1010C
1030
C_A
DIGITAL MASTERING REFORMATTER
1010D

FIG. 10